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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LAWRENCE R. YOUST
DANAMRAJ & YOUST, P.C.
5910 NORTH CENTRAL EXPRESSWAY
SUITE 1450
DALLAS, TX 75206

EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,193	PIERCE, JOHN L.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-11,13-16,20,23,24,27-35 and 37-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-11,13-16,20,23,24,27-35 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The declaration filed on 8-26-4 under 37 CFR 1.131 is sufficient to overcome the Hirashima reference.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 9, 32-34 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama (6018462) and Blumberg (6387830).

At column 1, lines 44-57; column 2, lines 1-4; column 2, line 30 to column 3, line 15; and column 4, lines 15-19, Sakuyama discloses (Previously amended) A method of producing a wafer-interposer comprising the steps of: attaching one or more first electrical contacts 3 to a lower surface of a substrate 1 comprising a material; attaching one or more second electrical contacts 4 to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts (illustrated in FIG. 1); and creating one or more first electrical pathways 5 passing through the substrate and connecting the first electrical contacts to the second electrical contacts; wherein the first and

second electrical contacts are connection pads; mounting the substrate on a semiconductor wafer 6a including at least one semiconductor die 6a; wherein the step of mounting the substrate on the semiconductor wafer further comprises the step of depositing a conductor 8 on at least one third electrical contact 7 on an upper surface of the semiconductor wafer, the at least one third electrical contact being associated with the at least one semiconductor die; aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the at least one third electrical contact correspond with the first electrical contacts on the lower surface of the substrate; mounting the substrate on a semiconductor wafer including at a least one semiconductor die; attaching the substrate and semiconductor wafer assembly to a testing apparatus "device"; and testing a portion of the at least one semiconductor die; wherein the step of testing the portion of the at least one semiconductor die further comprises performing parametric "electrical characteristics" testing on at least one of the dies; wherein the step of testing the portion of least one semiconductor die inherently further comprises testing the semiconductor dies simultaneously; and grading "testing" one or more performance "electrical" characteristics of each semiconductor die during testing.

To further clarify the disclosure wherein the step of testing the portion of the at least one semiconductor die inherently further comprises testing

the semiconductor dies simultaneously, it is noted that the apparent antecedent basis for the language "the semiconductor dies" is "at least one semiconductor die," and, as applied to the rejection, Sakuyama discloses one semiconductor die. Furthermore, the step of testing the one semiconductor die of Sakuyama inherently further comprises testing the semiconductor die simultaneously with everything that exists or occurs at the same time.

However, Sakuyama does not appear to explicitly disclose that the substrate comprises a B-stage adhesive material.

Nonetheless, at column 2, lines 41-49; column 4, lines 27-36; and column 5, lines 24-56, Blumberg discloses a substrate 100 comprising a B-stage adhesive material. Moreover, it would have been obvious to combine this disclosure of Blumberg with the disclosure of Sakuyama because it would facilitate provision of the substrate of Sakuyama.

In the alternative, claims 8, 9, 32-34 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama and Blumberg as applied to claims 8, 9, 32-34 and 37-40, and further in combination with Horiuchi.

Sakuyama and Blumberg do not appear to explicitly disclose the second electrical contacts having greater surface area and greater pitch than the first electrical contacts.

Notwithstanding, at column 1, lines 6-18 and 31-67; column 2, lines 9-16; column 3, lines 41-50; column 3, line 58 to column 4, line 3; column 5, lines 27-31; column 6, line 49 to column 8, line 39; and column 9, lines 24-26, Horiuchi discloses second electrical contacts 28 having greater surface area and greater pitch than first electrical contacts 22. In addition, it would have been obvious to combine this disclosure of Horiuchi with the disclosure of Sakuyama and Blumberg because, as taught by Horiuchi as cited, it would cheaply provide a semiconductor device that is light in weight and small in size, meeting the demand for fabricating semiconductor chips in small sizes.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama and Blumberg; or Sakuyama, Blumberg and Horiuchi, as applied to claim 32, and further in combination with Tsai (6489180).

Sakuyama, Blumberg and Horiuchi do not appear to explicitly disclose wherein the step of mounting the substrate on the semiconductor wafer further comprises the step applying a layer of no-flow underfill to the upper surface of the semiconductor wafer.

Nevertheless, at column 2, lines 5-8, Tsai discloses wherein a step of mounting a substrate 120 on a semiconductor wafer 110 further comprises a step applying a layer of no-flow underfill 130 to the upper surface of the semiconductor wafer. Furthermore, it would have been obvious to combine

the underfill of Tsai with the disclosure of the applied prior art because it would help prevent short-circuits.

In the alternative, claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama and Blumberg; or Sakuyama, Blumberg and Horiuchi as applied to claims 38-40 supra, and further in combination with Kline (6483043).

Sakuyama, Blumberg and Horiuchi do not appear to explicitly disclose wherein the step of testing the portion of the at least one semiconductor die further comprises performing parametric testing on at least one of the dies; wherein the step of testing the portion of at least one semiconductor die further comprises testing the semiconductor dies simultaneously; and grading one or more performance characteristics of each semiconductor die during testing.

Still, at column 6, lines 21-45, Kline discloses wherein a step of testing a portion of at least one semiconductor die further comprises performing parametric testing on at least one of the dies; wherein the step of testing the portion of at least one semiconductor die further comprises testing the semiconductor dies simultaneously; and grading one or more performance characteristics of each semiconductor die during testing. Additionally, it would have been obvious to combine this disclosure of Kline with the

disclosure of the applied prior art because it would facilitate the testing of the applied prior art.

Claims 10, 11, 15, 16, 20, 23, 24 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama (6018462), Blumberg (6387830) and Tsai (6489180).

As cited supra, Sakuyama discloses

10. (Currently amended) A method for producing a wafer-interposer assembly comprising the steps attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a material; attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts; creating one or more first electrical pathways passing through the substrate and connecting the first electrical contacts to the second electrical contacts; depositing a conductor 8 on one or more third electrical contacts 7 on an upper surface of a semiconductor wafer 6a, the semiconductor wafer including one or more semiconductor dies 6a and the third electrical contacts being associated with the semiconductor dies; aligning the substrate with the semiconductor wafer so that the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate; attaching the substrate to the semiconductor wafer; wherein the first, second and third electrical

contacts are connection pads; wherein the step of attaching wafer comprises the steps of: placing the semiconductor wafer on a first flat surface 1 and holding the semiconductor wafer in place; placing the substrate on a second flat surface 6a and holding the substrate in place; and bringing the first and second flat surfaces together so that the semiconductor wafer and the substrate form an adhesive bond (via 8); inherently singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies; wherein each conductor is a solder ball; attaching the substrate and semiconductor wafer assembly to a testing apparatus "device"; and testing at least one of the semiconductor dies; wherein the step of testing the semiconductor dies further comprises performing parametric "electrical characteristics" testing on at least one of the dies; wherein the step of testing the semiconductor dies inherently further comprises testing the semiconductor dies simultaneously; grading "testing" one or more performance "electrical" characteristics of each semiconductor die during testing; inherently singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies; sorting "testing" the semiconductor die assemblies based on the one or more performance characteristics; and sorting the semiconductor die assemblies into conforming and nonconforming groups "testing."

To further clarify, Sakuyama discloses inherently singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies because the substrate and wafer assembly are singular; therefore, it is inherent that they are singulated.

To further clarify the disclosure wherein the step of testing the semiconductor dies inherently further comprises testing the semiconductor dies simultaneously, it is noted that the apparent antecedent basis for the language "the semiconductor dies" is "one or more semiconductor dies," and, as applied to the rejection, Sakuyama discloses one semiconductor die. Furthermore, the step of testing the one semiconductor die of Sakuyama inherently further comprises testing the semiconductor die simultaneously with everything that exists or occurs at the same time.

However, Sakuyama does not appear to explicitly disclose that the substrate comprises a B-stage adhesive material.

Nonetheless, at column 2, lines 41-49; column 4, lines 27-36; and column 5, lines 24-56, Blumberg discloses a substrate 100 comprising a B-stage adhesive material. Moreover, it would have been obvious to combine this disclosure of Blumberg with the disclosure of Sakuyama because it would facilitate provision of the substrate of Sakuyama.

Also, Sakuyama and Blumberg do not appear to explicitly disclose wherein the step of mounting the substrate on the semiconductor wafer

further comprises the step applying a layer of no-flow underfill to the upper surface of the semiconductor wafer.

Nevertheless, at column 2, lines 5-8, Tsai discloses wherein a step of mounting a substrate 120 on a semiconductor wafer 110 further comprises a step applying a layer of no-flow underfill 130 to the upper surface of the semiconductor wafer. Furthermore, it would have been obvious to combine the underfill of Tsai with the disclosure of Sakuyama and Blumberg because it would help prevent short-circuits.

Claims 10, 11, 13-16, 20, 23, 24 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama, Blumberg and Tsai as applied to claims 10, 11, 15, 16, 20, 23, 24 and 27-31, and further in combination with Horiuchi (6297553).

Sakuyama, Blumberg and Tsai do not appear to explicitly disclose second electrical contacts having greater surface area and greater pitch than the first electrical contacts; singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies; applying additional metalization to one or more of the third electrical contacts to redistribute them prior to the attachment of the substrate; and adding additional metalization to one or more of the third electrical contacts to improve the contact between the conductor and the third electrical contacts.

Regardless, as cited supra, Horiuchi discloses second electrical contacts having greater surface area and greater pitch than first electrical contacts; singulating a substrate 62 and semiconductor wafer 60 assembly "laminate" into one or more semiconductor die assemblies "semiconductor device"; applying additional metalization 20 to one or more third electrical contacts 16 to redistribute them prior to the attachment of the substrate; and adding additional metalization to one or more third electrical contacts to improve the contact between a conductor 14 and the third electrical contacts. In addition, it would have been obvious to combine this disclosure of Horiuchi with the disclosure of Sakuyama, Blumberg and Tsai because, as taught by Horiuchi as cited, it would cheaply provide a semiconductor device that is light in weight and small in size, meeting the demand for fabricating semiconductor chips in small sizes.

In the alternative, claims 24 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuyama, Blumberg and Tsai; or Sakuyama, Blumberg, Tsai and Horiuchi as applied to claims 24 and 27-31 supra, and further in combination with Kline (6483043).

Sakuyama, Blumberg, Tsai and Horiuchi do not appear to explicitly disclose wherein the step of testing the semiconductor dies further comprises performing parametric testing on at least one of the dies; wherein the step of testing the semiconductor dies further comprises testing the

semiconductor dies simultaneously; grading one or more performance characteristics of each semiconductor die during testing; sorting the semiconductor die assemblies based on the one or more performance characteristics; and sorting the semiconductor die assemblies into conforming and nonconforming groups.

Nonetheless, at column 6, lines 21-45, Kline discloses wherein a step of testing semiconductor dies further comprises performing parametric testing on at least one of the dies; wherein the step of testing the semiconductor dies further comprises testing the semiconductor dies simultaneously; grading one or more performance characteristics of each semiconductor die during testing; sorting semiconductor die assemblies based on the one or more performance characteristics; and sorting the semiconductor die assemblies into conforming and nonconforming groups. Moreover, it would have been obvious to combine this disclosure of Kline with the disclosure of the applied prior art because it would facilitate the testing of the applied prior art.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
4-Feb-06